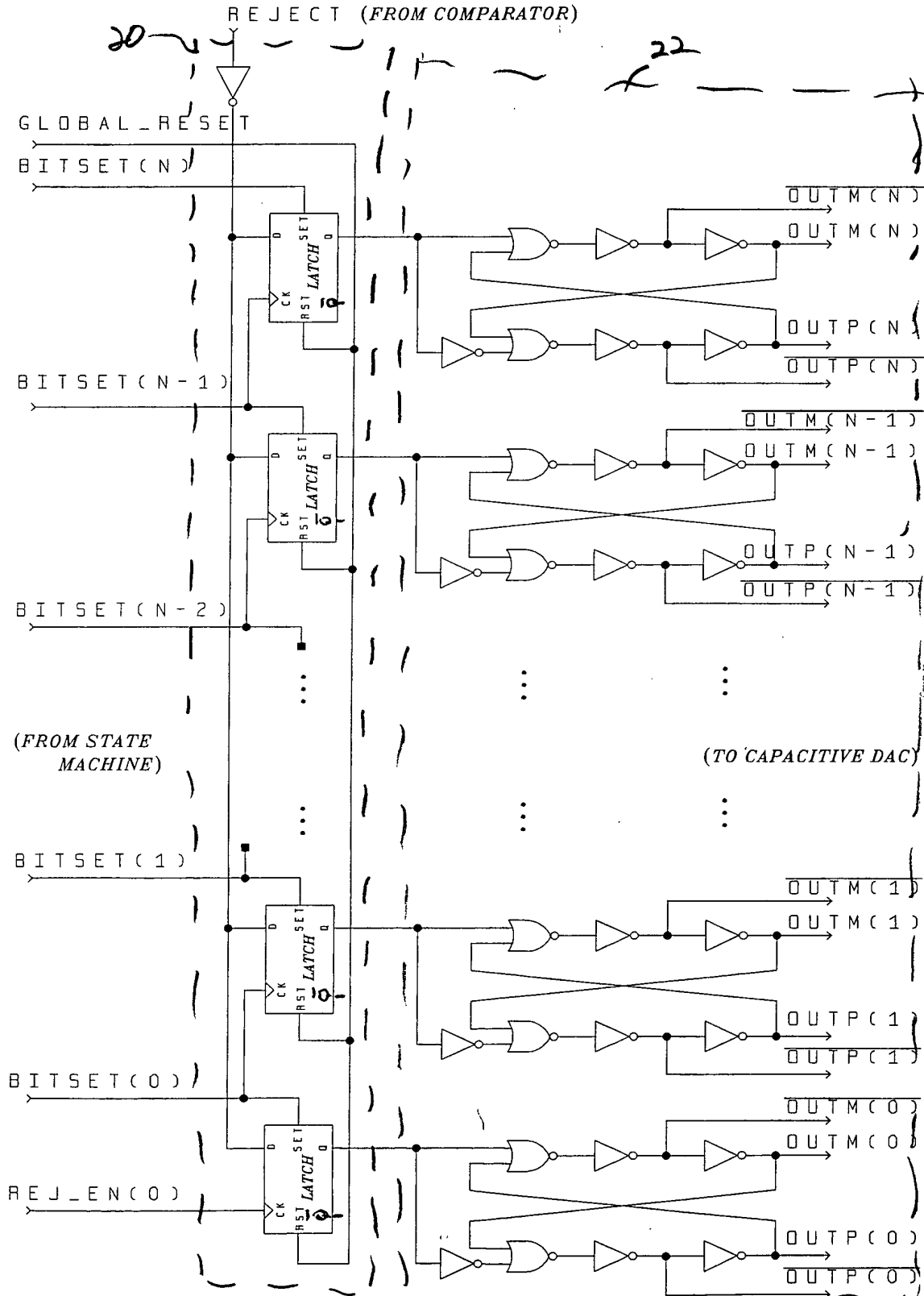


Fig. 1 (Prior Art)



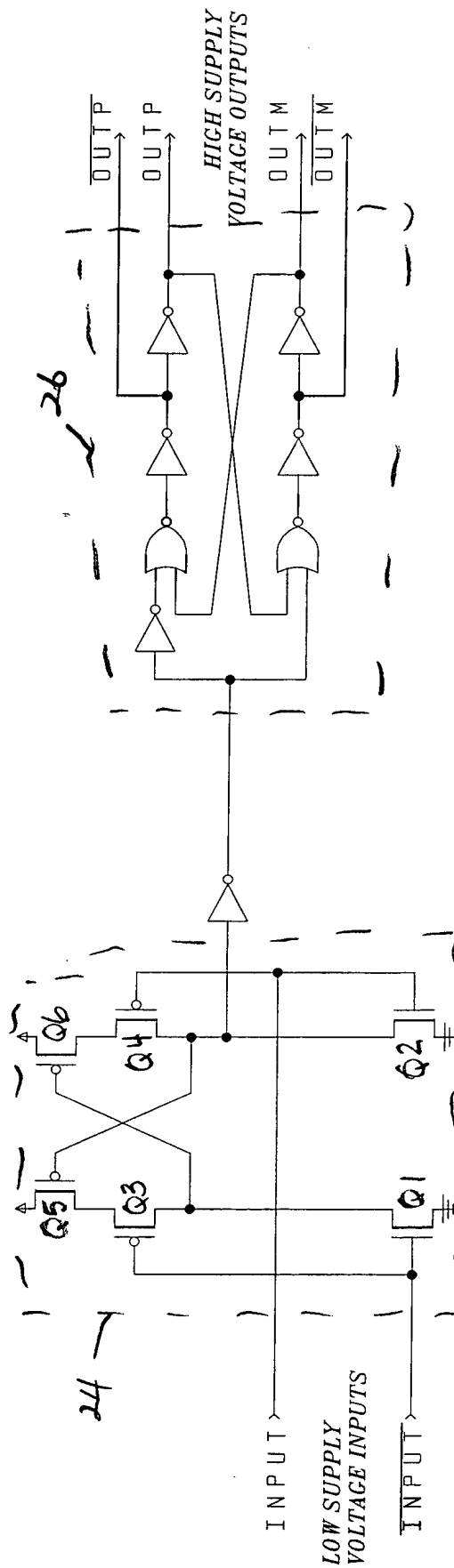


Fig. 3 (Prior Art)

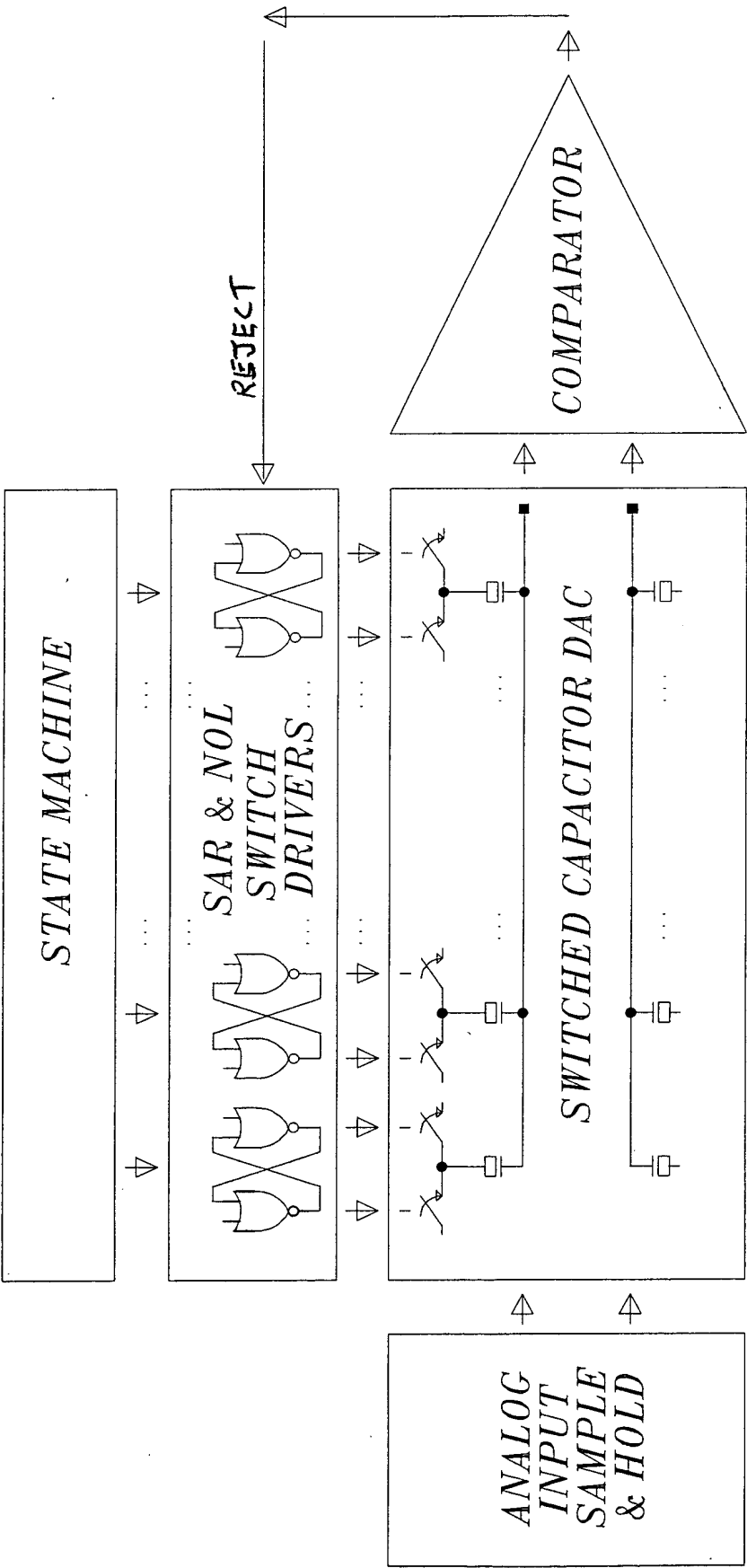


Fig. 4

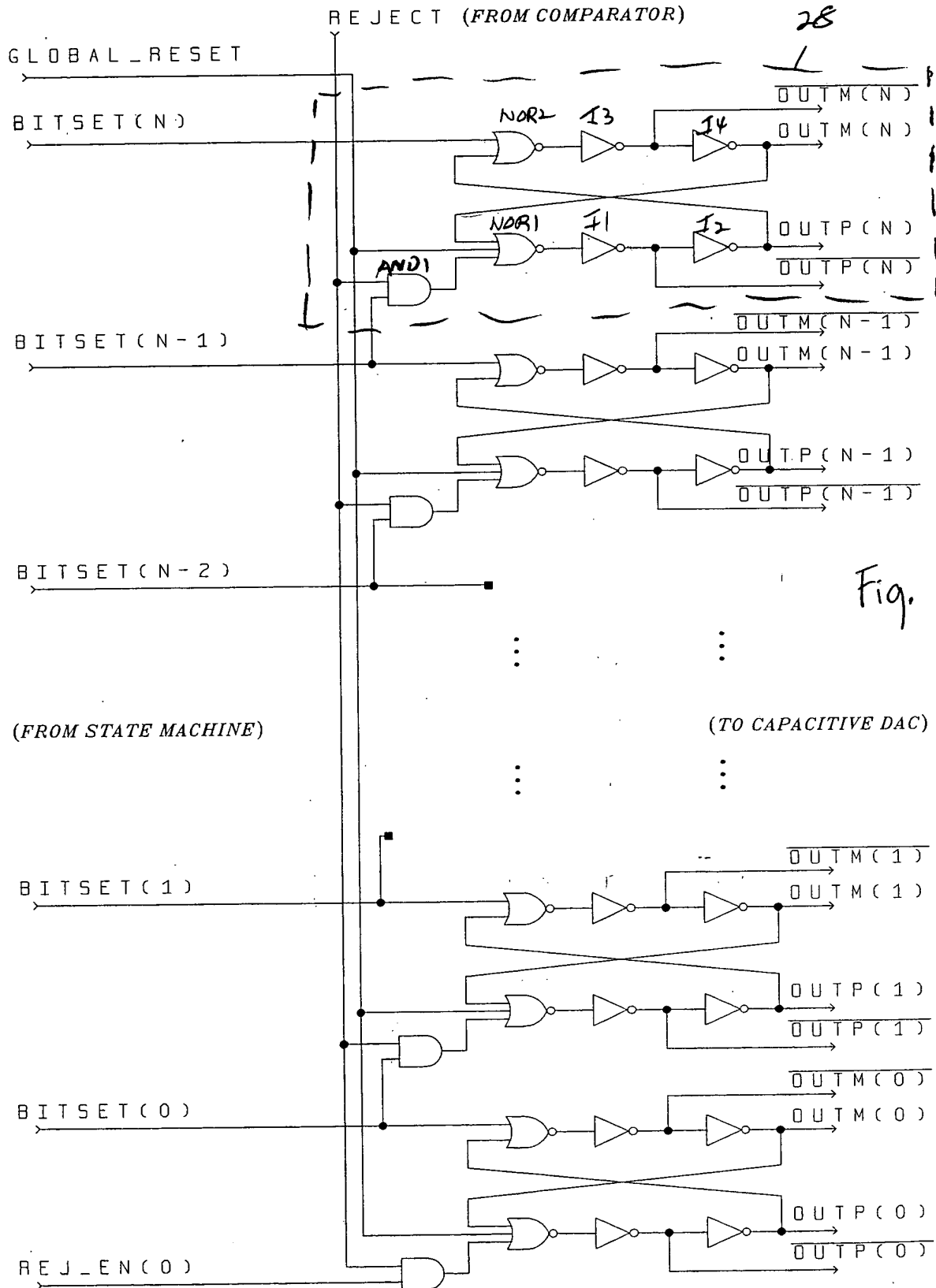


Fig. 5

NOR BASED
 SET-RESET
 LATCH

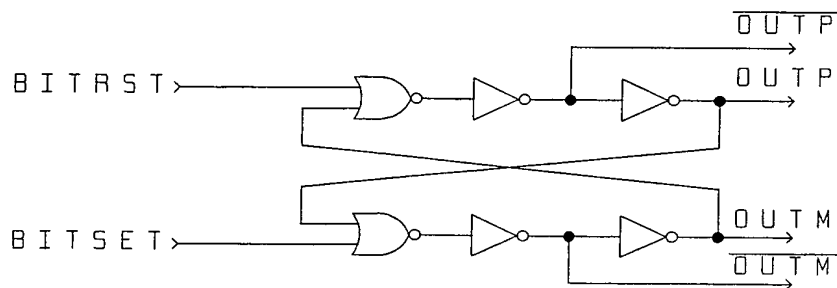


Fig. 6a

NAND BASED
 SET-RESET
 LATCH

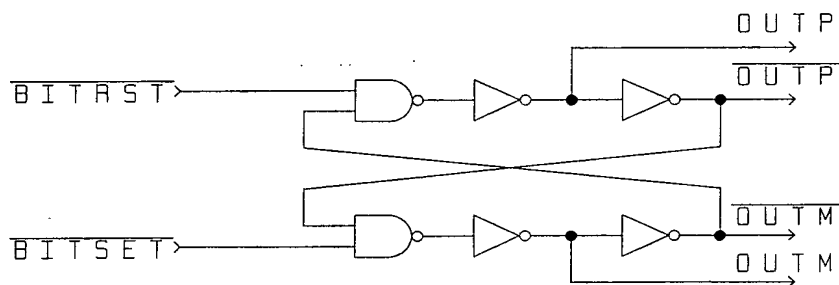


Fig. 6b

NAND BASED
 SET-RESET
 LATCH WITH
 SET & RST
 ENABLES

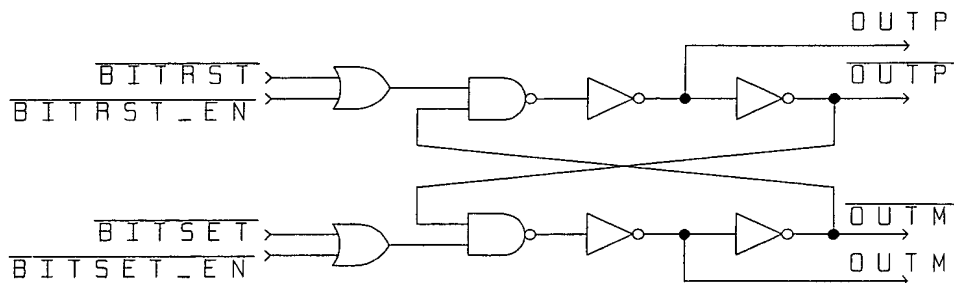


Fig. 6c

*NOR BASED
 SET-RESET
 LATCH WITH
 RST ENABLE
 & GLOBAL RST*

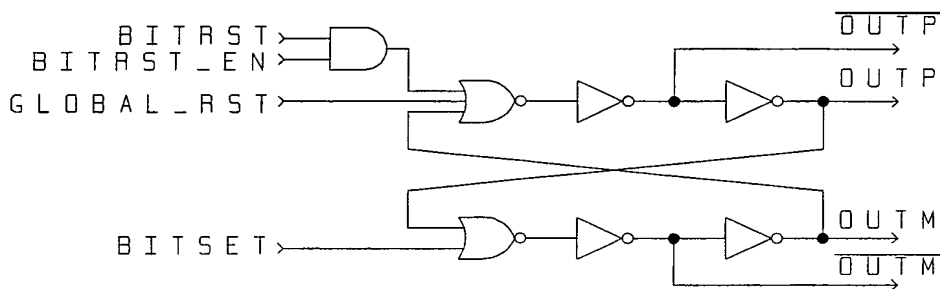


Fig. 6d

*NOR BASED
 SET-RESET
 LATCH WITH
 RST ENABLE
 & GLOBAL
 RST USING
 COMPOUND
 AOI GATE*

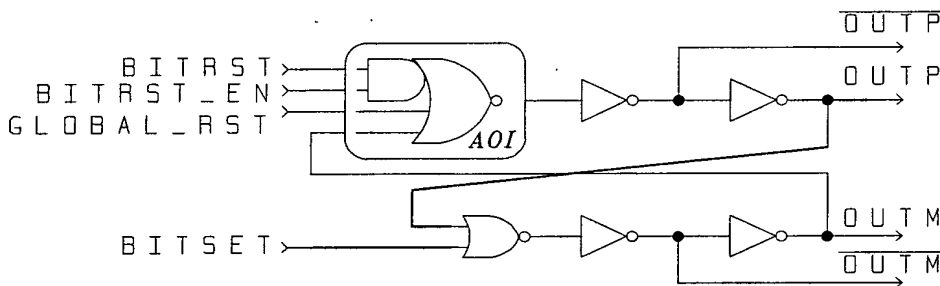


Fig. 6e

*NOR BASED
 SET-RESET
 LATCH WITH
 RST ENABLE
 & GLOBAL
 SET & RST
 USING
 COMPOUND
 AOI GATE*

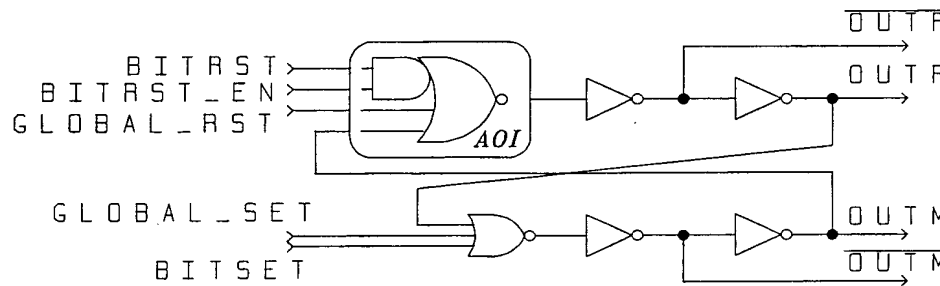


Fig. 6f

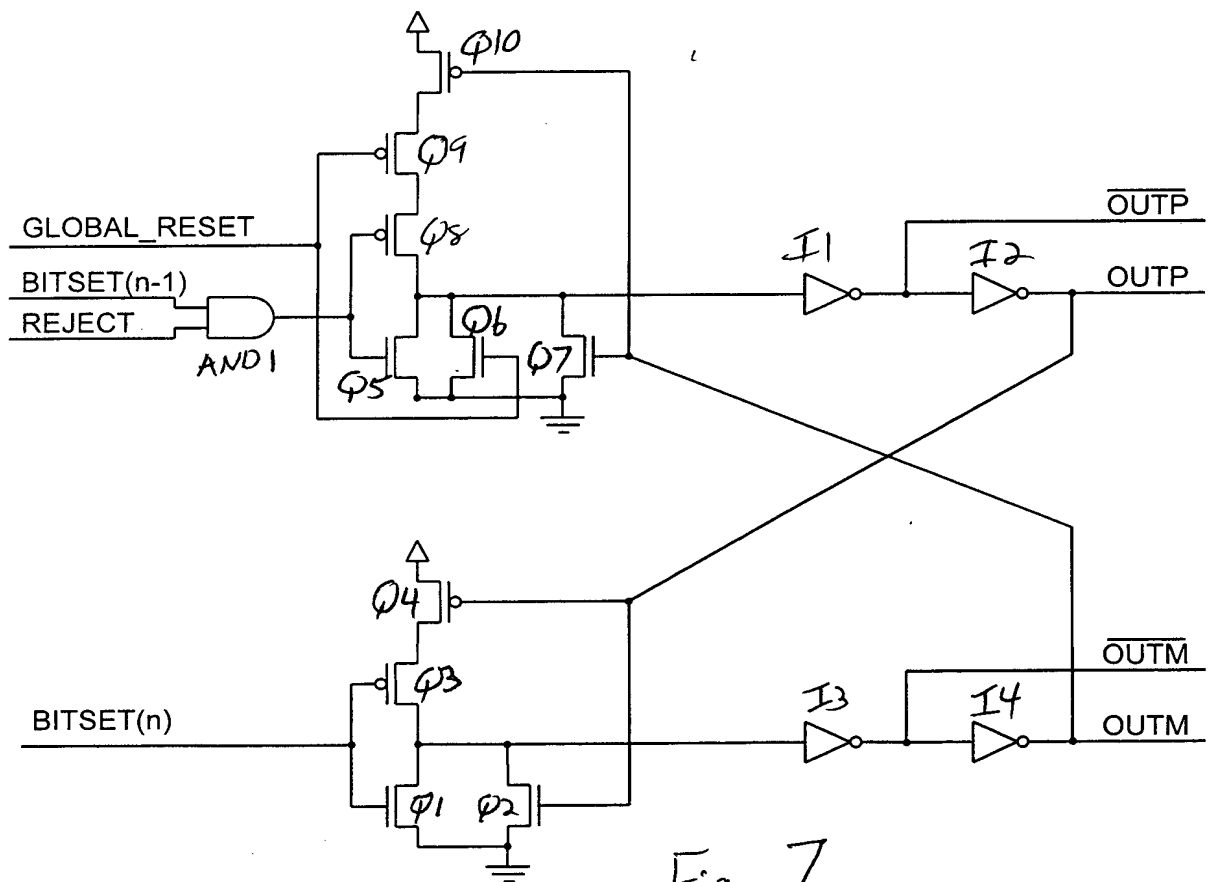
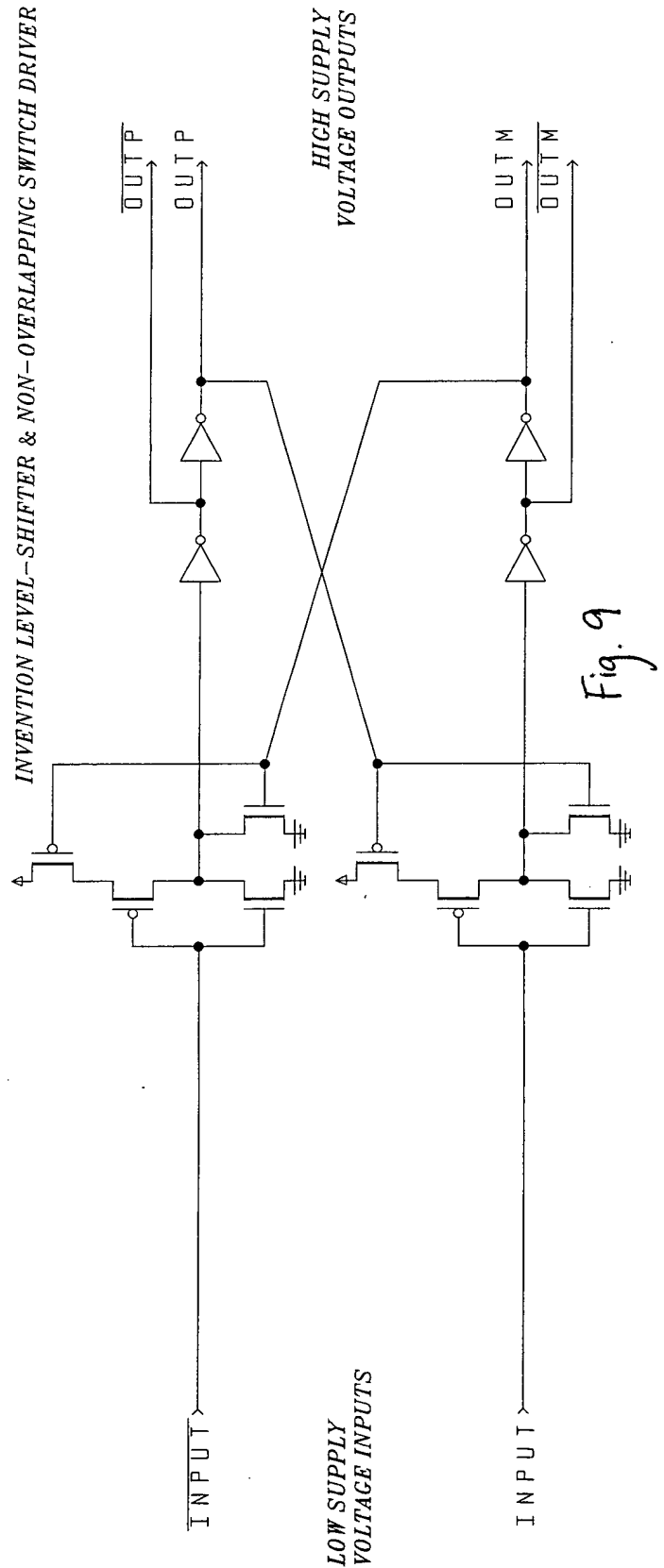
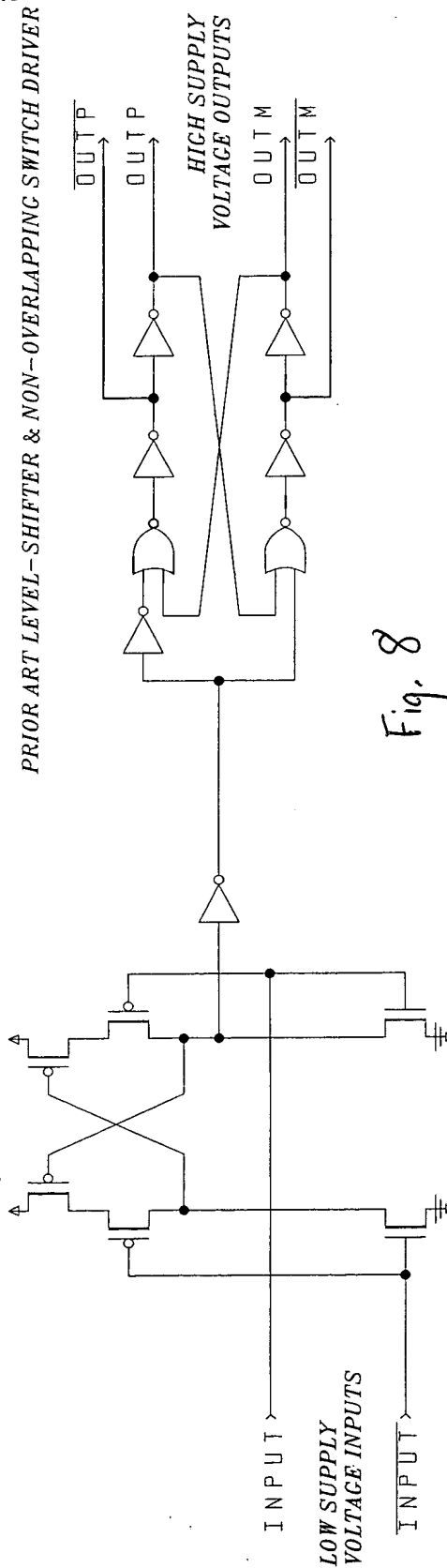


Fig. 7



PRIOR ART LATCH & NON-OVERLAPPING SWITCH DRIVER

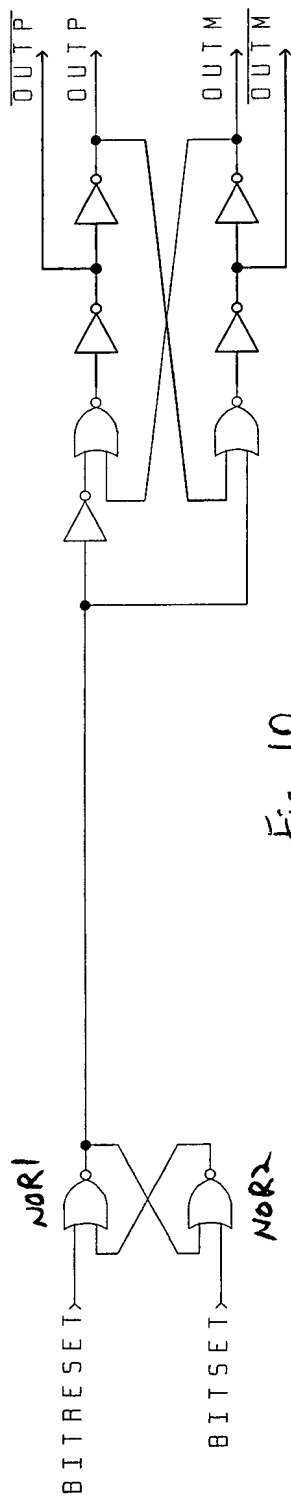


Fig. 10

INVENTION LATCH & NON-OVERLAPPING SWITCH DRIVER

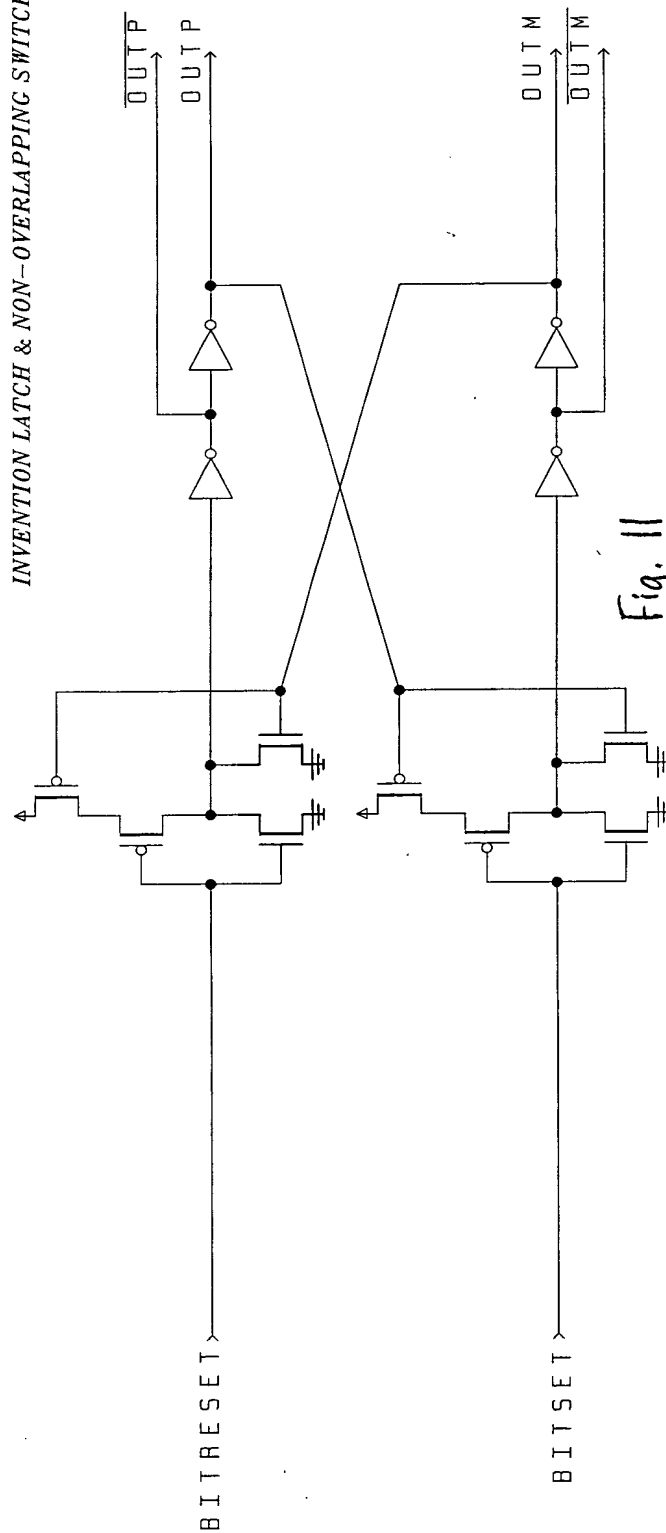


Fig. 11

